Short Papers

MESFET Simulation Oriented Toward Computer-Aided Microwave Circuit Design

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Abstract—**This paper describes a MESFET simulator designed to link physically based transistor simulation to microwave circuit simulation within an integrated CAD environment. The key features of the simulator are efficient implementation of a large-signal time-domain device simulation kernel; incorporation of extensive postprocessing of raw time-domain data; and an interactive, graphics-oriented user interface. An example is presented that demonstrates the utility of the approach for assessing circuit models.**

I. Introduction

The conventional information flow in semiconductor CAD is from process simulation, through device simulation, to circuit simulation. Fully integrated CAD systems are now feasible, but inefficient information transfer between individual simulators has hindered integration of the overall design process. The goal of the work described in this paper is to establish improved links between device simulation and circuit simulation. This motivation overlaps that of work described recently by Ghione *et al.* [1], but the emphasis, implementation techniques, and applications of the present work are different.

II. Philosophy and Implementation

The device information required for circuit simulation is the value of a device's terminal currents at any given time as a function of its terminal voltages at that time and all previous times, i.e.,

$$I_n(t) = f[V_1(t'), \cdots, V_m(t')] \qquad (1)$$

where m is the number of device terminals, $1 \leqslant n \leqslant m$, $-\infty < t' \leqslant t$, and the V_n are defined relative to some fixed potential. The present work exploits the observation that large-signal time-domain simulators calculate information in the form of (1) and that circuit models represent approximate subsets of this information. An adequately general and accurate large-signal time-domain simulator can therefore be used as a reference standard to evaluate the accuracy of circuit models and can be used instead of measurements as a source of data for calculating numerical values of parameters required by circuit models. This type of simulation also permits circuit design studies to start prior to fabrication and experimental characterization of devices.

There is no fundamental difficulty in implementing time-domain simulations of transistors. Reiser demonstrated the basic concept more than 15 years ago [2]; Hockney *et al.* [3] and Snowden [4] are among those who have made more recent contributions, and PISCES [5] is a well-known simulator with time-domain capabilities. The main drawback to using time-domain simulation has been computational intensity. The present work is an extension of Reiser's approach oriented toward efficient execution and the exploitation of modern computer hardware and software environments.

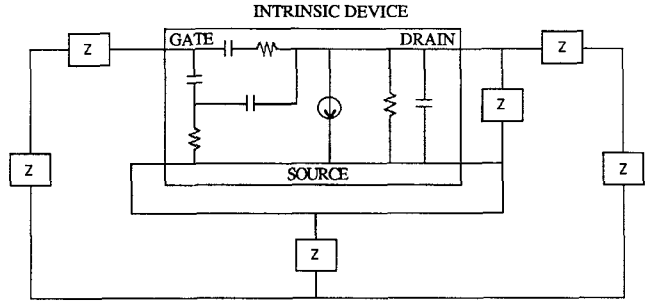

Fig 1. General equivalent circuit model for intrinsic MESFET's Several popular circuit models are obtained by deleting elements from this general circuit. The circuit topology for the specification of parasitic elements surrounding a two-port intrinsic device is also shown

A two-dimensional simulator, called BETTSI, has been developed. The most basic version of BETTSI is based on the drift-diffusion approximation.[1] Poisson's equation and the electron continuity equation are solved decoupled within a time step. Poisson's equation is solved using fully modified incomplete Choleski decomposition with conjugate gradient acceleration (MICCG). The electron continuity equation is solved using an asymmetrical nine-point physically based differencing scheme. The system of equations that results is solved iteratively using an incomplete LU decomposition preconditioner with biconjugate gradient acceleration.

Internal scheduling is incorporated for calculation of single-bias-point dc solutions, dc $I-V$ characteristics, small-signal admittance data via Fourier analysis of the current responses to voltage steps [7] (see the Appendix), periodic current responses to periodic voltage excitation, and terminal current transients for specified time-dependent terminal voltages. Small-signal postprocessing options are provided for devices configured as two-port networks. Small-signal current gain, stability factor, maximum available gain (MAG), maximum stable power gain (MSG), and unilateral available power gain are calculated as functions of frequency. The unity current gain (cutoff) frequency f_T and maximum frequency of oscillation $f_{\max}$ are calculated directly from the admittance matrix data. The small-signal admittance data may be transformed into impedance, hybrid, or scattering parameter representations.

BETTSI incorporates a small-signal equivalent circuit model optimizer. This calculates values for the elements of the intrinsic MESFET small-signal equivalent circuit model shown in Fig. 1,

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[1]Code which provides a Monte Carlo based scattering process level description of electron transport has also been completed and the inclusion of transport models of intermediate complexity [6] is planned.

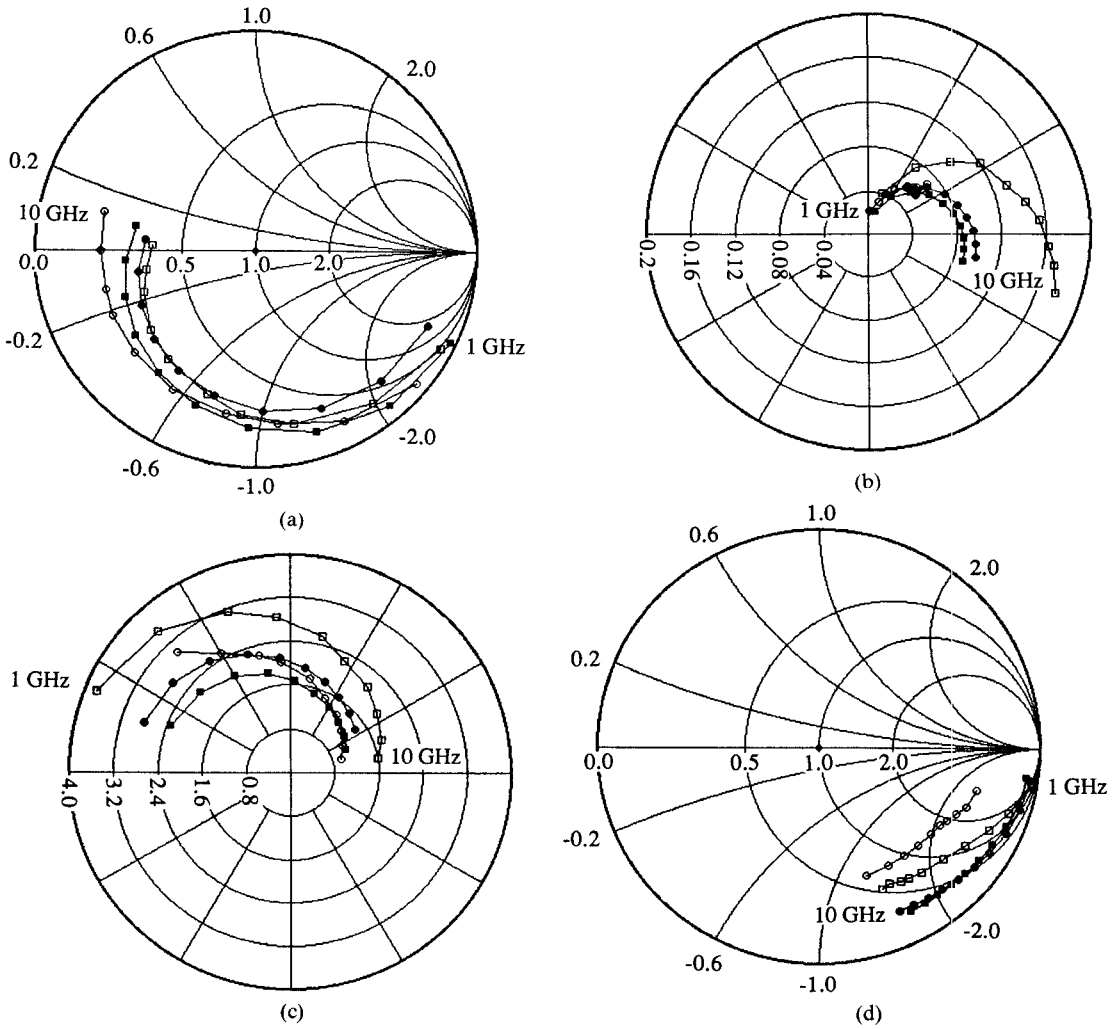

Fig. 2. Small-signal S parameters for a GaAs MESFET plotted on an impedance Smith chart (a) S_{11}, (b) S_{12} (c) S_{21}, (d) S_{22} ○ = experimental results from [8]; □ = theoretical results from [9]; ● = set A, computed by BETTSI using the velocity–field relation from [9], ■ = set B, computed by BETTSI using the velocity–field relation from [10]. $Z_0 = 50\ \Omega$, device width = 600 μm. Frequency range: 1–10 GHz. DC operating point: $V_{gs} = -2.0$ V, $V_{ds} = 6.0$ V. (Device length = 5.1 μm, gate length = 1.7 μm centered, epitaxial layer depth = 0.3 μm, epitaxial layer doping = 7.5×10^{16} cm^{-3}.)

providing the best least-squares fit to calculated small-signal data over a user-specified frequency range. Different weights may be assigned to the fits of individual two-port network parameters. Users may delete elements or change the dependence of the current source. Element removal reduces the equivalent circuit of Fig. 1 to any of several different equivalent circuits for intrinsic MESFET's which have appeared in the literature. The optimizer can therefore be used to parameterize a range of different models currently used in circuit design, and comparisons of the quality of the fit provided by the different models are easily performed. The model shown in Fig. 1 incorporates user-specified passive parasitics. Each parasitic impedance element (Z) in Fig. 1 has the form of a resistance in series with a reactance, where the reactance is either a capacitor or an inductor. Individual resistances and reactances may be set equal to zero. BETTSI performs the transformations between intrinsic and extrinsic device characteristics.

III. An Example Application

This example illustrates the use of BETTSI for investigating the validity of an approximate analytical circuit model. The MESFET that was modeled is a structure characterized experimentally by Willing, Rauscher, and de Santis [8] and modeled using an analytical approximation by Madjar and Rosenbaum [9]. Fig. 2 shows two sets of small-signal S-parameter results calculated using BETTSI. Set A uses the velocity–field relation suggested by Madjar and Rosenbaum [9] (saturated velocity = 1.36×10^7 cm/s, no negative differential mobility). Set B uses a more realistic velocity–field characteristic, an analytic form from Constant *et al.* [10] which includes negative differential mobility and a more realistic saturated velocity of 8×10^6 cm/s. The parasitic values suggested by Madjar and Rosenbaum [9] were used for both sets of results calculated using BETTSI. Fig. 2 also includes experimental results from [8] and the theoretical results from [9].

The differences between the set A results and the Madjar and Rosenbaum results are due primarily to the approximations in the Madjar and Rosenbaum model other than the use of an idealized velocity–field characteristic. The differences between the set A and set B results isolate the impact of the idealized velocity–field characteristic. In all cases except S_{22} the results from BETTSI are closer to the experimental values given in [8] than the results from the analytical model [9]. The Madjar and Rosenbaum model clearly captures the main features of device operation, however.

At low frequency the values of S_{21} predicted by BETTSI (set B) have a smaller magnitude than the measured values. This is because at low frequencies S_{21} is proportional to the transconductance, and transport models which do not account for electron velocity overshoot effects in GaAs (such as the drift-diffusion version of BETTSI used in this example) underestimate the transconductance [11].

IV. Discussion

Making data from device simulations available to circuit simulators in the form required by circuit simulators, and automating this process, are important CAD issues. Different types of circuit designs have different requirements. The present simulator is extremely effective for small-signal applications. BETTSI can provide a direct interface to pertinent circuit simulators, e.g. in calculating small-signal parameters for use by TOUCHSTONE or SUPERCOMPACT. Large-signal nonlinear microwave circuit design techniques are less well established. Harmonic balance techniques based on large-signal equivalent circuits are widely used, but physically based large-signal time-domain simulation is becoming an increasingly viable alternative for many situations. Single frequency periodic large-signal RF characterization can use generalized large-signal admittance matrices in which individual admittances are functions of the amplitudes and phases of the voltages on all device terminals. Such characterization permits power optimized design of oscillators and amplifiers (see e.g. [12]). Large-signal S parameters may also be calculated directly, although their utility is restricted to the same extent as measured large-signal S parameters. Another approach which uses time-domain simulation is mixed-mode simulation, in which terminal voltages, used as boundary conditions in the device simulator, evolve self-consistently as determined by a circuit simulator, which in turn obtains terminal currents from the device simulation. Bias elements with long time constants must normally be omitted, however, due to constants on CPU time.

V. Conclusions

The implementation and use of a physically based large-signal time-domain device simulator have been described. The goal of the work is to make device simulation more useful in CAD environments used by circuit designers. The central concepts of the work are the use of large-signal time-domain simulation and the inclusion of extensive postprocessing within the device simulator framework.

Appendix
The Geometric Capacitance Matrix

The Fourier decomposition small-signal step response method is widely considered to have the drawback that it is difficult to model the conduction current spike at $t = 0^+$ [7]. This appendix explains how the problem is overcome using a geometric capacitance matrix

The method is a generalization of a technique used previously in diode modeling [13]. The basic idea is to decompose the terminal currents at any instant in time into two components: one due to the motion of charges with terminal voltages held constant, and one due to changes in terminal voltages with charges held stationary. The exact equivalent circuit for the second component of current is the "geometric" ("cold" or "feedthrough") capacitance matrix. This matrix is calculated from solutions of Laplace's equation for the particular device geometry. Fourier analysis of the terminal current waveforms with the initial displacement current spike neglected provides a partial small-signal admittance representation. Surrounding the partial representation with the elements of the geometric capacitance matrix leads to the complete small-signal representation (Fig. 3).

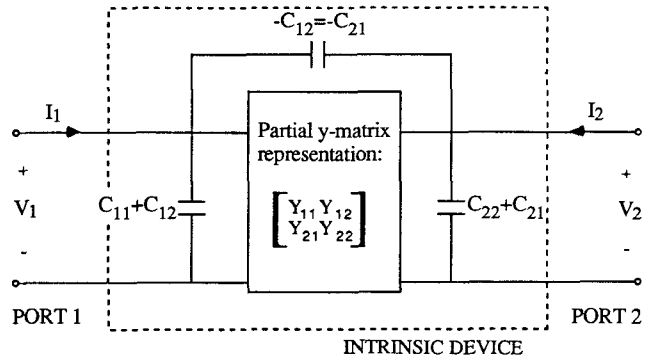

Fig. 3. Addition of the geometric capacitance matrix elements in a two-port representation. All subscripts refer to port numbers. $C_{ij} = Q_i/V_j$ when $V_k = 0$, $k \neq j$ where Q_i is the charge associated with the ith port.

The correctness of the geometric capacitance matrix formulation has been confirmed by direct comparisons with time-domain results obtained (i) with small sinusoidal excitations and (ii) with ramp excitations.

The geometric capacitance matrix has additional uses. It provides the basis for a simple and efficient implementation of the device–circuit interaction in mixed-mode simulation. A special case of this is the imposition of current boundary conditions. The techniques involved are straightforward extensions of those described previously for diodes [13].

Acknowledgment

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Jacobian Calculation Using the Multidimensional Fast Fourier Transform in the Harmonic Balance Analysis of Nonlinear Circuits

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Abstract **— A technique is developed whereby the gradient of frequency-domain simulation variables may be analytically determined using time-domain derivative information and the multidimensional fast Fourier transform. It is shown that this technique can be efficiently implemented when a circuit is driven by any number of incommensurate input frequencies. A harmonic balance simulator is constructed which uses this technique to determine the entries of the Jacobian matrix which are needed in a quasi-Newton iteration scheme. A significant reduction of simulation time is observed when compared with a harmonic balance simulator that uses matrix-multiplication-based transforms.**

I. INTRODUCTION

In the harmonic balance method of nonlinear analog circuit simulation, the linear subcircuit is analyzed in the frequency domain and the nonlinear subcircuit in the time domain. For simulations with multifrequency excitation, the time-domain and frequency-domain analyses have been interfaced using either the almost periodic discrete Fourier transform (APDFT) method [1], [2] or the multidimensional fast Fourier transform (NFFT) method [3]. The advantage of the APDFT is that computer implementation is relatively simple for an arbitrary number of incommensurate input frequencies. On the other hand the NFFT algorithm is computationally more efficient and exhibits superior numerical stability. An alternative method to that used by Rizzoli *et al.* [3] is presented here in which the Jacobian is calculated using the NFFT. This method has the advantage that frequency-domain derivatives may be computed for every frequency contained in the transform. It can also be used in conjunction with the block Newton iteration scheme [4].

II. HARMONIC BALANCE

Harmonic balance analysis proceeds by first selecting a set of frequency-domain analysis variables at every edge/node which is common to both the linear and nonlinear portions of the circuit. The frequency-domain independent variable is $\boldsymbol{X}$, and for impedance (admittance) type elements $\boldsymbol{X}$ is a set of current (voltage) phasors, while the dependent variable, $\boldsymbol{Y}$, is a set of voltage (current) phasors. Lowercase variables will be used to indicate time-domain quantities.

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The independent and dependent variables at a single node or edge will be denoted by the subscript n. Absence of this subscript will indicate the collection of *all* independent or dependent variables in the simulation. For example, $\boldsymbol{X}_n$ represents the frequency-domain independent variable containing all analysis frequencies at the nth node/edge, and $\boldsymbol{y}$ is the collection of the time-domain dependent variables at *every* node/edge and sample time.

The objective of the harmonic balance procedure is to "balance" the response of the nonlinear elements ($\boldsymbol{Y}$) to that of the linear elements ($\tilde{\boldsymbol{Y}}$). Defining the forward and inverse transform operators as $\mathcal{F}$ and $\mathcal{F}^{-1}$ respectively, the "balance point" is determined iteratively as follows. During each iteration and at each analysis node/edge an updated estimate of $\boldsymbol{X}_n$ is inverse Fourier transformed into the time domain,

$$\boldsymbol{x}_n = \mathcal{F}^{-1}(\boldsymbol{X}_n) \tag{1}$$

and applied as input to the constitutive relations of a nonlinear element. This yields the time-domain response ($\boldsymbol{y}_n$) for the present iterate of the dependent variable:

$$\boldsymbol{y}_n = \boldsymbol{h}(\boldsymbol{x}_n). \tag{2}$$

This is then Fourier transformed to the frequency domain,

$$\boldsymbol{Y}_n = \mathcal{F}(\boldsymbol{y}_n) \tag{3}$$

and compared with the response of the linear circuit to generate the error function E, $E = \|\boldsymbol{E}\|$ where $\boldsymbol{E} = [E_{k,n}] = [Y_{k,n} - \tilde{Y}_{k,n}]$; the subscript k denotes the frequencies and n the edges/nodes of elements $E_{k,n}$ of the matrix $\boldsymbol{E}$.

The error function is minimized by iteratively selecting better estimates for all independent variables. Generally, methods using first derivative information, known as quasi-Newton methods, are preferred. For each iteration the updated version of all independent variables is calculated using

$$^{\iota+1}\boldsymbol{X} = {}^{\iota}\boldsymbol{X} - ({}^{\iota}\boldsymbol{J}^{-1})({}^{\iota}\boldsymbol{E}) \tag{4}$$

where the leading superscript is the iteration index and ${}^{\iota}\boldsymbol{J} = {}^{\iota}(\partial \boldsymbol{E}/\partial \boldsymbol{X})$ is the Jacobian matrix or an approximation to the Jacobian matrix.

III. NFFT

The harmonic balance algorithm can be generalized to signals having N incommensurate input frequencies by using a multidimensional Fourier transform. The operations in (1) and (3) then become

$$x_{\boldsymbol{m},n} = \frac{1}{|\boldsymbol{M}|} \sum_{k_1=0}^{M_1-1} \sum_{k_2=0}^{M_2-1} \cdots \sum_{k_N=0}^{M_N-1} X_{k,n} \cdot \exp \frac{2\pi}{j} \left(\frac{k_1}{M_1} m_1 + \frac{k_2}{M_2} m_2 + \cdots + \frac{k_N}{M_N} m_N \right) \tag{5}$$

and

$$Y_{\boldsymbol{k},n} = \sum_{m_1=0}^{M_1-1} \sum_{m_2=0}^{M_2-1} \cdots \sum_{m_N=0}^{M_N-1} y_{\boldsymbol{m},n} \cdot \exp 2j\pi \left(\frac{m_1}{M_1} k_1 + \frac{m_2}{M_2} k_2 + \cdots + \frac{m_N}{M_N} k_N \right) \tag{6}$$

where $|\boldsymbol{M}| = \Pi^N |M_i|$ and the subscripts $\boldsymbol{k}$ and $\boldsymbol{m}$ are multi-indices which represent $[k_1 k_2 \cdots k_N]$ and $[m_1 m_2 \cdots m_N]$ respec-

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